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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/699,077	10/27/2000	Masahiro Ishida	KPO089	9031

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EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	3

DATE MAILED: 11/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/699,077	ISHIDA ET AL.	
	Examiner	Art Unit	
	Ayal I Sharon	2123	

-- The MAILING DATE of this communicati n appears on th c ver sheet with the c rrespondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Introduction

1. Claims 1-12 of U.S. Application 09/699,077 filed on 10/27/2000 are presented for examination. The application has a foreign priority date of 01/24/2000.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

   A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

   Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,461,882. Although the conflicting claims are not identical, they are not patentably distinct from each other because both claim fault simulation methods for integrated circuits, comprising the steps of: 1) generating a test pattern

sequence, 2) performing a "transition"/"logic value sequence" simulation, and 3) generating a list of faults detectable by transient power supply current testing.

4. Claim 3 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2 of U.S. Patent No. 6,461,882. Although the conflicting claims are not identical, they are not patentably distinct from each other because both claim fault simulation methods for integrated circuits, comprising the steps of: 1) generating a gate delay fault, 2) checking whether the logic signal value sequence in an output signal of the line has changed, and if so, 3) registering the fault in the fault list.
5. Claim 5 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 3 of U.S. Patent No. 6,461,882. Although the conflicting claims are not identical, they are not patentably distinct from each other because both claim fault simulation methods for integrated circuits, comprising the steps of: 1) generating a signal line fault, 2) checking whether the logic signal value sequence in an output signal of the line has changed, and if so, 3) registering the fault in the fault list.
6. Claim 7 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 4 of U.S. Patent No. 6,461,882. Although the conflicting claims are not identical, they are not patentably distinct from each other because both claim fault simulation methods for integrated circuits, comprising the steps of: 1) generating a path delay fault, 2)

checking whether the logic signal value sequence in an output signal of the line has changed, and if so, 3) registering the fault in the fault list.

7. Claims 10 and 12 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 5 of U.S. Patent No. 6,461,882. Although the conflicting claims are not identical, they are not patentably distinct from each other because they all claim a fault simulator for integrated circuits, comprising the steps of: 1) generating a test pattern sequence, 2) performing a "transition"/"logic value sequence" simulation, and 3) generating a list of faults detectable by transient power supply current testing. (Note: Claim 10 in the application also claims a "memory for storing the results of step 2), which is inherent because otherwise the results of step 2) would be lost. Claim 12 in the application also claims a "fault inserting means for inserting the fault into said semiconductor IC", which is also inherent, because otherwise the fault is not inserted into the system and the validation cannot be performed.)

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The prior art used for these rejections is as follows:

10. Ooshima et al., U.S. Patent 5,321,354. (Henceforth referred to as "**Ooshima**").

11. Liu et al., U.S. Patent 5,425,036. (Henceforth referred to as "**Liu**").

12. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

13. **Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ooshima in view of Liu.**

14. In regards to Claim 1, Ooshima teaches the following limitations of Claim 1:

> 1. A fault simulation method for a semiconductor IC, said method comprising the steps of:
> generating a test pattern sequence composed of two or more test patterns for input to said semiconductor IC;
> (Ooshima, especially: col.4, lines 1-20)
>
> ... in the case of applying thereto each of said two or more test patterns of said test pattern sequence, and calculating a logic signal value sequence in each signal line in said semiconductor IC; and
> (Ooshima, especially: col.4, lines 20-61)
>
> generating a list of faults, which are detectable by a transient power supply current testing using said test pattern sequence, through the use of said logic signal value sequence in said each signal line calculated by said logic simulation.
> (Ooshima, especially: col.11, line 60 to col.12, line 10)

However, Ooshima does not expressly teach:

> performing a logic simulation of the operation of said semiconductor IC

Liu, on the other hand, teaches both the simulation and the emulation of a target system (See Fig.1, Items 142, 144, 200), as well as the target system itself (Fig.1, Item 300). As well as the inputting and outputting test vectors (Fig.1, Item 12) to and from the simulation.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Ooshima with those of Liu, because "the circuit verification step is typically accomplished through simulation, which serves to test the correctness of the circuit's functional behavior in

response to various applied stimuli, such as digital input signals or test vector patterns." (Liu, col.1, lines 29-35).

15. In regards to Claim 2, Ooshima teaches the following limitations of Claim 2:

2. The method of claim 1, wherein said fault list generating step is a step of generating said fault list for each logic-gate in said semiconductor IC.
(Ooshima, especially: col.4, line 20 to col.7, line 10;
summary on col.7, lines 3-10)

16. In regards to Claim 3, Ooshima teaches the following limitations of Claim 3:

3. The method of claim 2, wherein said fault list generating step is a step of checking, for said each logic gate, whether a logic signal value sequence in an output signal line of said each logic gate has been changed, and if so, generating said fault list in which an identifier of a test pattern sequence having changed said logic signal value sequence and said logic gate are registered in correspondence with each other.
(Ooshima, especially: col.4, line 20 to col.7, line 10;
summary on col.7, lines 3-10)

17. In regards to Claim 4, Ooshima teaches the following limitations of Claim 4:

4. The method of claim 1, wherein said fault list generating step is a step of generating said fault list for said each signal line.
(Ooshima, especially: col.4, line 20 to col.7, line 10;
summary on col.7, lines 3-10)

18. In regards to Claim 5, Ooshima teaches the following limitations of Claim 5:

5. The method of claim 4, wherein said fault list generating step comprising the steps of:
checking, for said each signal line, whether said logic signal value sequence in said each signal line has been changed;
(Ooshima, especially: col.4, line 20 to col.7, line 10;
summary on col.7, lines 3-10)

if so, checking whether a logic signal value sequence in an output signal line of a logic gate having its input connected to said signal line, in which said logic signal value sequence has been changed, is changed by a test pattern sequence having changed said logic signal value sequence in said signal line, and if so, generating said fault list in which said signal line and an identifier of said test pattern sequence having changed said logic signal value sequence in said signal line are registered in correspondence with each other.
(Ooshima, especially: col.4, line 20 to col.7, line 10;
summary on col.7, lines 3-10)

19. In regards to Claim 6, Ooshima teaches the following limitations of Claim 6:

6. The method of claim 1, wherein said fault list generating step is a step of generating said fault list for each signal propagation path in said semiconductor IC.
(Ooshima, especially: col.4, line 20 to col.7, line 10;
summary on col.7, lines 3-10)

20. In regards to Claim 7, Ooshima teaches the following limitations of Claim 7:

7. The method of claim 6, wherein said fault list generating step is a step of checking, for said each signal propagation path, whether logic signal value sequences at respective points in said each signal propagation path have all been changed, and if so, generating said fault list in which an identifier of a test pattern sequence having changed said logic signal value sequences and said each signal propagation path are registered in correspondence with each other.
(Ooshima, especially: col.4, line 20 to col.7, line 10;
summary on col.7, lines 3-10)

21. In regards to Claim 8, Ooshima teaches the following limitations of Claim 8:

8. The method of claim 1, further comprising the step of calculating said logic signal value sequence for every test pattern sequence prior to said fault list generating step.
(Ooshima, especially: col.4, line 20 to col.7, line 10;
summary on col.7, lines 3-10)

22. In regards to Claim 9, Ooshima teaches the following limitations of Claim 9:

9. The method of claim 1, further comprising the step of calculating said logic signal value sequence and generating said fault list upon generation of each test pattern sequence.
(Ooshima, especially: col.4, line 20 to col.7, line 10;
summary on col.7, lines 3-10)

23. In regards to Claim 10, Ooshima teaches the following limitations of Claim 10:

10. A fault simulator for a semiconductor IC, comprising:
test pattern generating means for generating a test pattern sequence composed of two or more test patterns for input to said semiconductor IC;
(Ooshima, especially: col.4, lines 1-20)

a logic simulator supplied with said test pattern sequence, for performing a logic simulation of the operation of said semiconductor IC in the case of applying thereto each of said two or more test patterns, and for calculating and outputting a logic signal value sequence in each signal line in said semiconductor IC;
(Ooshima, especially: col.4, lines 20-61)

a memory for storing said calculated logic signal value sequence generated in said each signal line for each test pattern sequence; and
(Ooshima, especially: col.4, lines 20-61)

fault list generating means supplied with said logic signal value sequence of said each signal line stored in said memory, for generating a list of faults detectable by a transient power supply current testing using said test pattern sequence.
(Ooshima, especially: col.11, line 60 to col.12, line 10)

24. In regards to Claim 11, Ooshima teaches the following limitations of Claim 11:

11. A fault simulation method for a semiconductor IC, said method comprising the steps of:
inserting an assumed fault in said semiconductor IC;
(Ooshima, especially: col.4, lines 1-20)

generating a test pattern sequence composed of two or more test patterns for input to said semiconductor IC;
(Ooshima, especially: col.4, lines 20-61)

applying said test pattern to said semiconductor IC with said assumed fault inserted therein and performing a circuit simulation of the operation of said semiconductor IC to thereby calculate a transient power supply current of said semiconductor IC;
(Ooshima, especially: col.4, lines 20-61)

comparing said calculated transient power supply current with the transient power supply current of a normal circuit and deciding whether said assumed fault is detectable by a transient power supply current testing using said test pattern sequence; and
(Ooshima, especially: col.11, line 60 to col.12, line 10)

generating a fault list in which said detectable fault and an identifier of said test pattern sequence are registered.
(Ooshima, especially: col.11, line 60 to col.12, line 10)

25. In regards to Claim 12, Ooshima teaches the following limitations of Claim 12:

12. A fault simulator for a semiconductor IC comprising:
test pattern generating means for generating a test pattern sequence composed of two or more test patterns for input to said semiconductor IC;
(Ooshima, especially: col.4, lines 1-20)

fault inserting means for inserting an assumed fault into said semiconductor IC;
(Ooshima, especially: col.4, lines 20-61)

a circuit simulator for applying said test pattern to said semiconductor IC with said assumed fault inserted therein and performing a circuit simulation of the operation of said semiconductor IC to thereby calculate a transient power supply current of said semiconductor IC;
(Ooshima, especially: col.11, line 60 to col.12, line 10)

and fault list generating means for comparing said calculated transient power supply current with the transient power supply current of a normal circuit, for deciding whether said assumed fault is detectable by a transient power supply current testing using said test pattern sequence, and for registering said detectable fault and an identifier of said test pattern sequence in a fault list.
(Ooshima, especially: col.11, line 60 to col.12, line 10)

Conclusion

26. The following prior art has been found to be pertinent to the claimed invention.

Patents

27. Beasley et al. U.S. Patent 5,483,170. See col.1-2. Describes the use of a single test vector for testing ICs, and using only Idd current to analyze IC faults.

28. Burlison et al. U.S. Patent 5,552,744. See col.1-2. Describes a "High Speed Iddq Monitor Circuit."

29. Teene. U.S. Patent 5,726,997. See col.1. Describes monitoring Iddq current for testing purposes.

30. Sanada, U.S. Patent 5,850,404. See col.1, Figs.1A, 2A, 5. The prior art method of testing CMOS circuits is described in the background to the invention. Prior art includes test patterns and fault dictionaries.

31. Sakaguchi. U.S. Patent 5,949,798. See cols.1-2. The prior art method of testing CMOS circuits is described, including test patterns and monitoring supply current.

32. Fura, U.S. Patent 5,953,519. Teaches a method for generating hardware simulation models. See Fig.0

33. Cole, Jr. et al. U.S. Patent 6,031,386. Teaches a method of testing ICs by measuring transient voltage. See Abstract.

34. Vu et al. U.S. Patent 6,140,832. See col.1-2. Describes the monitoring of Iddq current for testing of CMOS circuits.

35. Cox et al. U.S. Patent 6,163,763. Teaches testing of Simulated circuit. See "Background Art", col.1-2.

36. Gattiker et al. U.S. Patent 6,175,244. See col.1. The prior art method of testing VLSI circuits is described, including test vectors and monitoring power supply current.

37. Hollander. U.S. Patent 6,182,258. Teaches testing of Simulated circuit. See Fig.1, Item 38.

38. Hollander. U.S. Patent 6,347,388. Teaches testing of Simulated circuit. See Fig.1, Item 38.

39. Cortner et al. U.S. Patent 6,513,137. See col.1-2. Describes Iddt test approaches.

Published Articles

40. Beasley et al. "Idd Pulse Response Testing : A Unified Approach to Testing Digital and Analogue ICs." Electronics Letters. Nov. 25, 1993. pp.2101-2103.

41. Beasley et al. "Idd Pulse Response Testing on Analog and Digital CMOS Circuits." Proc. Int'l Test Conf, 1993. Oct. 21, 1993. pp.626-634.

42. Jiang, W. and Vinnakota, B. "IC Test Using the Energy Consumption Ratio." Proc. 36th ACM/IEEE DAC. 1999. pp.976-981.

43. Plusquellic, J.F. et al. "Digital IC Device Testing by Transient Signal Analysis (TSA)." Electronics Letters. Aug. 31, 1995. pp.1568-1570.

44. Plusquellic, J.F. et al. "Digital Integrated Circuit Testing Using Transient Signal Analysis." Proc. Int'l Test Conf, 1996. Oct. 25, 1996. pp.481-490.

45. Segura, J.A. "An Approach to Dynamic Power Consumption Current Testing of CMOS ICs." Proc. 13th IEEE VLSI Test Symposium, 1995. May 3, 1995. pp.95-100.

46. Shyang-Tai, Su et al. "Dynamic Power Supply Current Monitoring of SRAMs." Proc. 7th Annual IEEE Int'l ASIC Conf. and Exhibit, 1994. Sept. 23, 1994. pp.370-373.

47. Jian Liu, et al. "Power Supply Current Detectability of SRAM Defects." Proc. Of 4th Asian Test Symposium. Nov. 24, 1995. pp.367-373.

48. Makki, R. et al. "Transient Power Supply Current Testing of Digital CMOS Circuits." Proc. Int'l Test Conf, 1995. Oct. 25, 1996. pp.892-901.

49. Jian Liu, et al. "Dynamic Power Supply Current Testing of CMOS SRAMs." Proc. 7th Asian Test Symposium, 1998. Dec. 4, 1998. pp.348-353.

50. Agrawal, V. "Contest: A Concurrent Test Generator for Sequential Circuits." Proc. 25th ACM/IEEE DAC, 1988. 1988. pp.84-89.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (703) 306-0297. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703) 305-9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

4th floor receptionist's office
Crystal Park 2
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The fax phone numbers for the organization where this application or proceeding is assigned are:

All communications: (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is: (703) 305-3900.

Ayal I. Sharon

Art Unit 2123

October 31, 2003